PROCESSOR PIPELINE STALL APPARATUS AND METHOD OF OPERATION

ABSTRACT OF THE DISCLOSURE

There is disclosed a data processor for stalling the instruction execution pipeline after a cache miss and re-loading the correct cache data into any bypass devices before restarting the pipeline. The data processor comprises: 1) an instruction execution pipeline comprising N processing stages, each of the N processing stages performing one of a plurality of execution steps associated with a pending instruction being executed by the instruction execution pipeline; 2) a data cache for storing data values used by the pending instruction; 3) a plurality of architectural registers for receiving the data values from the data cache; 4) bypass circuitry for transferring a first data value from the data cache directly to a functional unit in one of the N processing stages without first storing the first data value in a destination one of the plurality of architectural registers; and 5) a cache refill controller for detecting that a cache miss has occurred at a first address associated with the first data value, receiving a missed cache line from a main memory coupled to the data processor, and causing the first data value to be transferred from the missed cache line to the functional unit.